REMARKS

Claims 1-46 are currently pending in the application. In the final office action prior to the filing of the Request for Continued Examination accompanying this amendment, claims 1-33 and 35-46 were finally rejected. Claim 34 was objected to. Claims 1, 22, and 38 have been amended herein.

The Examiner finally rejected claims 1-33 and 35-46 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2002/0049824 A1 (Wilson). The rejection is again respectfully traversed.

Wilson describes a multi-processor computer architecture having a distributed shared memory. The system includes a plurality of uniform memory access (UMA) cells 100 interconnected by an interconnect 20. Each UMA cell includes a processor 102 and a memory 104 which includes a memory controller 106. Each memory controller 106 includes a so-called "cache of history counter" (CofHC) 108. Each entry in CofHC 108 represents a page (indicated by page address field 112) in the associated memory 104 and includes a plurality of counters (e.g., 114-120 of Fig. 2). Each counter for a given entry tracks a different metric for the corresponding memory page. For example, each of counters 114, 115, and 116 corresponds to one of the other UMA's (e.g., 200, 300, etc.) in the system, and tracks the number of times the processor in the corresponding UMA accesses the memory page represented by that entry. Migration counter 118 is incremented upon each migration of the page represented by the CofHC from one cache to another. Write counter 120 is incremented for each write to the page. By tracking these metrics, the system can determine (i.e., using the decision tree 250 of Fig. 3) whether there is a more efficient memory location for a given page in memory. See paragraphs [0023]-[0030].

Significantly, none of the counters described by Wilson determines or tracks transaction latency or any period of time. That is, as described above, Wilson's counters track the number of

times specific types of events occur in the system, e.g., how many times a cached memory page is accessed by specific processors in the system, so that it can then determine whether the page should be moved or copied to another cache. None of the quantities counted represent a period of time, i.e., a latency. In fact, there is nothing in Wilson which tracks latency, particularly for individual system transactions, e.g., memory or I/O accesses. Therefore, none of Wilson's counters can be characterized as a latency counter.

By contrast, claim 1 of the present invention recites "a latency counter operable to generate a latency count for each of selected" memory transactions. That is, the recited latency counter maintains a count which is representative of the length of time (e.g., as measured in clock cycles) required to complete all or a portion of a particular memory or I/O transaction.

Claim 1 also recites "a plurality of histogram counters," each of which is "operable to count selected ones of the latency counts corresponding to an associated latency range." That is, each histogram counter tracks the number of transaction latencies (as determined by the latency counter) which fall within a particular latency range. For example, one histogram counter might be responsible for counting latency counts which fall within the range 600-700 clock cycles while another would be responsible for counting latency counts which fall within the range 700-800 clock cycles, and so on. So, not only does the invention recited in claim 1 include the tracking of latencies for specific memory transactions, it also includes a second level of counting (a counting of the latency counts), i.e., where each of these transaction latencies fits with respect to multiple ranges within an overall time window.

Wilson neither describes nor suggests the determination or tracking of any type of latency as recited in claim 1 of the present application. Wilson does note that the information collected by the CoHC counters may be used to determine whether a particular memory page should be replicated or migrated to a different memory location which, in turn, may result in improvements in system latency (see paragraph [0030]). However, Wilson does not discuss how or even

whether such latency improvements are determined. Latency measurements are clearly not performed or tracked using the CoHC counters or any of the other components of Wilson's system.

Even if one accepts that the CoHC counter may be characterized as generating a latency count as recited in the claims of the present application, Wilson still does not teach or suggest the tracking of how many such latency counts correspond to particular latency ranges. That is, Wilson also fails to show the use of histogram counters to count the latency counts as recited in claim 1.

The Examiner has referred to Wilson's history counters (i.e., CoHC 108 and 208 of Fig. 1) as corresponding to the "histogram counters" recited in the claims of the present application, despite the fact these same counters were also referred to as anticipating the "latency counter" recited in the claims. The Examiner also now refers to paragraph [0041] as if this qualifies as one of the "clearer reference areas" offered.

The "history counters" of Wilson, i.e., counters 114-120 in the cache of history counters (CofHC) 108, track the "history" of access and migrations for a particular page in memory. See [0027]-[0029]. Paragraph [0041] merely describes how these counters are initialized and incremented. None of the counters described in Wilson track the results of another counter, much less which counts fall into particular latency ranges. That is, even if one accepts the Examiner's position that Wilson's cache of history counters correspond to the latency counter recited in the claims of the present application, there simply is no teaching or suggestion in Wilson of another type of counter, i.e., a histogram counter, which provides a second level of counting beyond that provided by the latency counter, i.e., a counting of the latency counts.

The Examiner is inappropriately using the same teaching in Wilson (i.e., the CoHC counters) to reject two different limitations of the claims. Either they map to one or the other, but not both. Unless the Examiner can show a plurality of counters with the functionality of the

histogram counters recited in the claims, the rejection should be withdrawn.

Because Wilson fails to teach or suggest a latency counter which is operable to generate latency counts for transactions involving memory, and because Wilson also fails to teach or suggest a plurality of histogram counters for counting the latency counts for corresponding latency ranges, it is respectfully submitted that the rejection of the claims of the present application over Wilson is overcome.

Notwithstanding the foregoing, amendments have been proposed herein to more clearly describe the invention and to make the distinctions between the claimed invention and the teaching of Wilson more clear for the Examiner. Specifically, claims 1, 22, and 38 have each been amended to recite that each latency count represents "time required for completion of at least a portion of the corresponding transaction." These amendments are supported throughout the present specification such as, for example, at page 31, line 24 to page 32, line 16.

As discussed above, the claims are believed to be allowable in their present form without these amendments. Therefore, these clarifying amendments are being provided merely for the purpose of advancing prosecution of this application and not for any reason related to patentability.

The Applicants respectfully acknowledge the Examiner's indication of allowable subject matter in claim 34. However, in view of the foregoing, claim 34 is believed to be allowable without amendment.

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CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Joseph M. Villeneuve
Reg. No. 37,460

P.O. Box 70250
Oakland, California 94612-0250
(510) 663-1100